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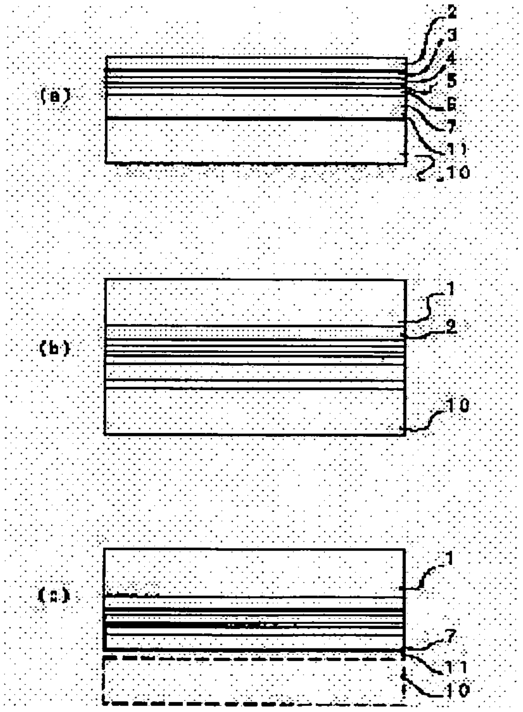
(54) FABRICATION OF SEMICONDUCTOR LIGHT EMITTING ELEMENT



(57)Abstract:

PROBLEM TO BE SOLVED: To prevent dopant from diffusing into an active layer during fabrication of a semiconductor light emitting element.

SOLUTION: A method for fabricating a semiconductor light emitting element comprises a step for forming a p-type semiconductor layer having single or a plurality of layers, a light emitting layer of AlGaInP based semiconductor material, and an n-type semiconductor layer sequentially on a nondoped GaAs substrate 10 before forming an n-type GaP thick film layer 1, and a step for removing the nondoped GaAs substrate 10. Since a transparent substrate semiconductor light emitting element is fabricated without using a p-type substrate and a thick film layer, p-type dopant is prevented from being diffused into an active layer during high temperature processing and high internal quantum efficiency is sustained resulting in a high brightness semiconductor light emitting element.

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CLAIMS

[Claim(s)]
[Claim 1] In the manufacture approach of a semi-conductor light emitting device of coming to carry out laminating formation of the semi-conductor layer on a substrate The process which carries out the laminating of the p type semiconductor layer which consists of a monolayer or two or more layers on a non dope mold GaAs substrate, The process which carries out the laminating of the luminous layer which consists of a monolayer of the semiconductor material of an AlGaInP system, or two or more layers on said p type semiconductor layer, The manufacture approach of the semi-conductor light emitting device characterized by having the process which carries out the laminating of the semi-conductor layer which consists of a monolayer of n mold, or two or more layers on said luminous layer, the process which forms an n mold GaP thick-film layer on said n-type-semiconductor layer, and the process which removes said non dope mold GaAs substrate.
[Claim 2] In the manufacture approach of a semi-conductor light emitting device of coming to carry out laminating formation of the semi-conductor layer on a substrate The process which carries out the laminating of the p type semiconductor layer which consists of a monolayer or two or more layers on an n mold GaAs substrate, The process which carries out the laminating of the luminous layer which consists of a monolayer of the semiconductor material of an AlGaInP system, or two or more layers on said p type semiconductor layer, The manufacture approach of the semi-conductor light emitting device characterized by having the process which carries out the laminating of the semi-conductor layer which consists of a monolayer of n mold, or two or more layers on said luminous layer, the process which forms an n mold GaP thick-film layer on said n-type-semiconductor layer, and the process which removes said n mold GaAs substrate.
[Claim 3] The stroke which forms said n mold GaP thick-film layer is the manufacture approach of the semi-conductor light emitting device according to claim 1 or 2 characterized by including the stroke which arranges an n mold GaP substrate on said n-type-semiconductor layer, and the stroke which joins said n mold GaP substrate to said n-type-semiconductor layer top face by high temperature processing.
[Claim 4] The stroke which forms said n mold GaP thick-film layer is the manufacture approach of the semi-conductor light emitting device according to claim 1 or 2 characterized by including the stroke which grows an n mold GaP growth phase epitaxially on said n-type-semiconductor layer.
[Claim 5] Said p type semiconductor layer which consists of a monolayer which carries out a laminating on said non dope mold or said n mold GaAs substrate, or two or more layers is the manufacture approach of the semi-conductor light emitting device according to claim 1 to 4 characterized by including a transparent current diffusion layer to the luminescence wavelength of the light from said luminous layer at least.
[Claim 6] Said current diffusion layer is the manufacture approach of the semi-conductor light emitting device according to claim 5 characterized by consisting of a monolayer chosen from an AlxGa1-xAs (0.6< x<0.9) layer, zIn(AlyGa1-y)1-zP (0<=y<=1, 0<=z<=1), and a GaP layer, or two or more layers.
[Claim 7] Said current diffusion layer is the manufacture approach of the semi-conductor light emitting device according to claim 6 characterized by forming said AlxGa1-xAs (0.6< x<0.9) layer at least on

said non dope mold or said n mold GaAs substrate after forming the aforementioned (AlyGa1-y) zIn1-zP (0<=y<=1, 0<=z<=1) layer or said GaP layer.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the manufacture approach of the semi-conductor light emitting device of high brightness about the manufacture approach of a semi-conductor light emitting device.
[0002]
[Description of the Prior Art] In recent years, the semi-conductor light emitting device is widely used for optical communication, an information-display panel, etc. It is important for these semi-conductor light emitting devices that it is high brightness. It is decided by internal quantum efficiency and external outgoing radiation effectiveness, the brightness, i.e., the effectiveness, of a semi-conductor light emitting device, among these external outgoing radiation effectiveness is greatly influenced by component structure.
[0003] Generally in the semi-conductor light emitting device, using a transparent substrate to luminescence wavelength is performed for the purpose of raising external outgoing radiation effectiveness. This is because light can be taken out not only from a top face but from four side faces, when a transparent substrate is used to luminescence wavelength to the ability to use only the outgoing radiation light to the top face of a semi-conductor light emitting device when an opaque substrate is used to luminescence wavelength. Moreover, the reflected light in the underside of a semi-conductor light emitting device also becomes possible [carrying out outgoing radiation from a top face and a side face], when a transparent substrate is used to luminescence wavelength.
[0004] The manufacture approach using a transparent substrate is applied to the red or the infrared semi-conductor light emitting device using the semiconductor material of the infrared semi-conductor light emitting device and AlGaAs system which used the semiconductor material of an InGaAsP system, the yellow semi-conductor light emitting device using the semiconductor material of a GaAsP system, the green semi-conductor light emitting device using the semiconductor material of a GaP system, etc. to this luminescence wavelength.
[0005] On the other hand, in the semi-conductor light emitting device of an AlGaInP system, what is indicated by JP,6-296040,A is known as the manufacture approach using a transparent substrate to luminescence wavelength. As the manufacture approach of this conventional semi-conductor light emitting device is shown in drawing 5 (a) or (b) Two or more semi-conductor layers 55 which contain a luminous layer 53 on the opaque GaAs substrate 51 to luminescence wavelength are grown epitaxially. Wafer junction of the GaAs substrate 51 and the GaP substrate 58 which carried out epitaxial growth formation of two or more semi-conductor layers 55 which contain a luminous layer 53 on the top face by besides performing an arrangement postheat treatment for the transparent GaP substrate 58 to luminescence wavelength is carried out. Furthermore, the opaque GaAs substrate 51 is removed to luminescence wavelength, and a semi-conductor light emitting device is obtained.
[0006] Moreover, what is indicated by JP,6-302857,A is known as other manufacture approaches in the semi-conductor light emitting device of an AlGaInP system. The manufacture approach of the other

conventional semi-conductor light emitting devices As shown in drawing 6 (a) thru/or (c), two or more semi-conductor layers 65 which contain a luminous layer 63 on the opaque GaAs substrate 61 to luminescence wavelength are grown epitaxially. Several 10 micrometers grows the GaP current diffusion layer 66 after that, wafer junction of the GaP substrate 68 is carried out by performing an arrangement postheat treatment in the field which removed and removed the opaque GaAs substrate 61 to luminescence wavelength, and a semi-conductor light emitting device is obtained. In this case, the GaP current diffusion layer 66 which grows on a luminous layer is balance with the mechanical strength of the epitaxial growth phase 67 after removing growth time amount and the GaAs substrate 61, and, generally is about 50-100 micrometers. This is because growth time amount becomes it long that they are a crack and 100 micrometers or more which becomes empty and the cost of a semi-conductor light emitting device becomes high, when dealing with the epitaxial growth phase 67 after removing the GaAs substrate 61 as it is 50 micrometers or less.

[0007]

[Problem(s) to be Solved by the Invention] There was a trouble [as / as is shown below] in the manufacture approach of the above-mentioned conventional semi-conductor light emitting device.

[0008] (1) Grow a luminous layer epitaxially on an opaque GaAs substrate to luminescence wavelength. Wafer junction of the GaAs substrate and GaP substrate which formed the epitaxial growth phase in the top face by besides performing an arrangement postheat treatment for a transparent GaP substrate to luminescence wavelength is carried out. Furthermore, in the case of the manufacture approach of removing an opaque GaAs substrate to luminescence wavelength, it is necessary to use either as p mold substrate among transparent GaP substrates to an opaque GaAs substrate and luminescence wavelength to luminescence wavelength.

[0009] However, p mold substrate had to dope p mold dopants (for example, Zn, Mg, etc.) about [1x1019cm -] three in order to usually make resistivity low, and since the diffusion coefficient of p mold dopant was large, the dopant was spread in the luminous layer at the time of epitaxial growth or high temperature processing of wafer junction, the decline in internal quantum efficiency arose, and it had the trouble that the brightness of a semi-conductor light emitting device fell.

[0010] (2) Grow a luminous layer epitaxially on an opaque GaAs substrate to luminescence wavelength. Several 10 micrometers grows a GaP current diffusion layer after that, and an opaque GaAs substrate is removed to luminescence wavelength. By the manufacture approach of carrying out wafer junction by performing an arrangement postheat treatment, a GaP substrate to the removed field Several 10-micrometer quite thin substrate needed to be dealt with, and there was a trouble that the yield fell, by the wafer crack at the time of mass production after removing a GaAs substrate until it joined the GaP substrate.

[0011] (3) moreover, the trouble of the above (2) -- in addition, since several 10-micrometer GaP current diffusion layer was p mold when n mold was used for a GaAs substrate, the total amount of a dopant increased more than the case where a several micrometers current diffusion layer is formed, and the dopant had the trouble of becoming easy to be spread, to the luminous layer as a result.

[0012] (4) On the other hand, since there are many amounts of dopants of a p mold GaAs substrate compared with an n mold GaAs substrate when p mold is used for a GaAs substrate in addition to the trouble of the above (2), dopant diffusion increases further. Consequently, the decline in luminous efficiency arose and the trouble of becoming small had the effectiveness which transposes an optical absorption substrate to a transparence substrate.

[0013] Luminescence from a barrier layer is added to the top face of a chip, and the object of this invention can be taken out also from a side face, and is to provide controlling diffusion of the dopant to a barrier layer with the semi-conductor light emitting device of ** and high brightness.

[0014]

[Means for Solving the Problem] This invention was made in view of the above-mentioned trouble, and the semi-conductor light emitting device of invention concerning claim 1 in the manufacture approach of a semi-conductor light emitting device In the manufacture approach of a semi-conductor light emitting device of coming to carry out laminating formation of the semi-conductor layer on a substrate The process which carries out the laminating of the p type semiconductor layer which consists of a monolayer or two or more layers on a non dope mold GaAs substrate, The process which carries out the laminating of the luminous layer which consists of a monolayer of the semiconductor material of an AlGaInP system, or two or more layers on a p type semiconductor layer, It is characterized by having the process which carries out the laminating of the semi-conductor layer which consists of a monolayer of n mold, or two or more layers on a luminous layer, the process which forms an n mold GaP thick-film layer on a n-type-semiconductor layer, and the process which removes a non dope mold GaAs substrate.

[0015] According to the above-mentioned configuration, since p mold substrate is not used, it becomes possible to control the diffusion to the barrier layer of p mold dopant at the time of high temperature processing, to maintain high internal quantum efficiency, and to obtain the semi-conductor light emitting device of high brightness.

[0016] Moreover, the semi-conductor light emitting device of invention concerning claim 2 In the manufacture approach of a semi-conductor light emitting device of coming to carry out laminating formation of the semi-conductor layer on a substrate The process which carries out the laminating of the p type semiconductor layer which consists of a monolayer or two or more layers on an n mold GaAs substrate, The process which carries out the laminating of the luminous layer which consists of a monolayer of the semiconductor material of an AlGaInP system, or two or more layers on a p type semiconductor layer, It is characterized by having the process which carries out the laminating of the semi-conductor layer which consists of a monolayer of n mold, or two or more layers on a luminous layer, the process which forms an n mold GaP thick-film layer on a n-type-semiconductor layer, and the process which removes an n mold GaAs substrate.

[0017] According to the above-mentioned configuration, since p mold substrate is not used, it becomes possible to control the diffusion to the barrier layer of p mold dopant at the time of high temperature processing, to maintain high internal quantum efficiency, and to obtain the semi-conductor light emitting device of high brightness. Furthermore, since diffusion of p mold dopant to the GaAs substrate from the p type semiconductor layer which grows epitaxially on an n mold GaAs substrate since a GaAs substrate is n mold is controlled, the ohmic contact of p mold electrode is easy to be obtained, and since the resistivity of a p type semiconductor layer is also maintained low, it becomes possible to obtain a semi-conductor light emitting device with more low operating voltage.

[0018] Moreover, invention concerning claim 3 is characterized by the stroke which forms an n mold GaP thick-film layer including the stroke which arranges an n mold GaP substrate on a n-type-semiconductor layer, and the stroke which joins an n mold GaP substrate to a n-type-semiconductor layer top face by high temperature processing in the manufacture approach of claim 1 or the semi-conductor light emitting device concerning 2.

[0019] According to the above-mentioned configuration, since junction formation of the n mold GaP substrate is carried out by high temperature processing on the n-type-semiconductor layer top face, an n mold GaP substrate thick enough can be produced easily, and it becomes possible to prevent lowering of the processing yield by the wafer crack.

[0020] Moreover, invention concerning claim 4 is characterized by the stroke which forms an n mold GaP thick-film layer including the stroke which grows an n mold GaP growth phase epitaxially on a n-type-semiconductor layer in the manufacture approach of claim 1 or the semi-conductor light emitting device concerning 2.

[0021] Since according to the above-mentioned configuration the n mold GaP thick-film layer is formed with epitaxial growth on a n-type-semiconductor layer and a production process can be simplified compared with claim 3, it becomes possible to manufacture a semi-conductor light emitting device more efficiently.

[0022] Moreover, claim 5 or invention concerning 6 is set to the manufacture approach of claim 1 thru/or the semi-conductor light emitting device concerning 4. The p type semiconductor layer which consists of a monolayer which carries out a laminating on a non dope mold or an n mold GaAs substrate, or two or more layers It is characterized by including a transparent current diffusion layer to the luminescence wavelength of the light from a luminous layer at least. Furthermore, it is characterized by a current diffusion layer consisting of a monolayer chosen from an AlxGa1-xAs (0.6< x<0.9) layer, zIn (AlyGa1-y)1-zP (0<=y<=1, 0<=z<=1), and a GaP layer, or two or more layers.

[0023] According to the above-mentioned configuration, since it has the transparent current diffusion layer to the luminescence wavelength of the light from said luminous layer, it becomes possible to decrease the light which it becomes easy to diffuse the current from p mold electrode, and is absorbed by p mold electrode. Furthermore, it enables zIn(AlyGa1-y)1-zP (0<=y<=1, 0<=z<=1) and a GaP layer to improve moisture resistance, since there are few aluminum contents compared with an AlxGa1-xAs (0.6< x<0.9) layer.

[0024] Moreover, invention concerning claim 7 is characterized by forming an AlxGa1-xAs (0.6< x<0.9) layer at least (AlyGa1-y), on a non dope mold or an n mold GaAs substrate, after forming a zIn1-zP (0<=y<=1, 0<=z<=1) layer or a GaP layer in the manufacture approach of the semi-conductor light emitting device concerning claim 6.

[0025] According to the above-mentioned configuration, on a barrier layer, since the outside is further equipped with the zIn1-zP (0<=y<=1, 0<=z<=1) layer or the GaP layer at least (AlyGa1-y), it becomes possible an AlxGa1-xAs (0.6< x<0.9) layer and to improve moisture resistance compared with the case of an AlxGa1-xAs (0.6< x<0.9) layer monolayer.

[0026]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained with reference to a drawing.

[0027] (Gestalt of the 1st operation) Drawing 1 (a) thru/or (c) are drawings showing the semi-conductor light emitting device formed in the gestalt of operation of the 1st of this invention, and drawing 1 (a) is [a plan and drawing 1 (c) of a side elevation and drawing 1 (b)] bottom views.

[0028] The structure of the semi-conductor light emitting device 100 formed in the gestalt of the 1st operation For example, on the n mold GaP substrate 1 The n mold GaP cap layer 2, n mold 0.77In0.23P interlayer 3, (aluminum0.2Ga0.8) The laminating of the n mold aluminum0.5In0.5P cladding layer 4, p mold Ga0.5In0.5P barrier layer 5, the p mold aluminum0.5In0.5P cladding layer 6, and two or more semi-conductor layers of p mold aluminum0.68Ga0.32As current diffusion layer 7 grade is carried out one by one. And p mold electrode 8 of the circle configuration which consists of AuZn/Mo/Au, and four n mold electrodes 9 of a circle configuration which consist of AuSi(s) are formed in the vertical side of the semi-conductor light emitting device 100.

[0029] Next, the manufacture approach of the semi-conductor light emitting device in the gestalt of the 1st operation is explained to a detail.

[0030] Drawing 2 (a) thru/or (c) are process drawings showing the manufacture approach of a semi-conductor light emitting device of having used the gestalt of operation of the 1st of this invention.

[0031] As shown in drawing 2 (a), on the non dope mold GaAs substrate 10 The p mold GaAs buffer layer 11 (1 micrometer), The p mold aluminum0.68Ga0.32As current diffusion layer 7 (5 micrometers), the p mold aluminum0.5In0.5P cladding layer 6 (1 micrometer), p mold Ga0.5In0.5P barrier layer 5 (0.5 micrometers), the n mold aluminum0.5In0.5P cladding layer 4 (1 micrometer), Sequential growth of n mold (aluminum0.2Ga0.8) 0.77In0.23P interlayer 3 (0.15 micrometers), the n mold GaP cap layer 2 (1 micrometer), etc. is carried out for example, by the organic metal chemical-vapor-deposition method (MOCVD law). Moreover, as a p mold dopant, Zn, Mg, etc. are used, for example. In addition, as the growth approach, various approaches, such as molecular beam epitaxy (MBE law) and organic metal molecular beam epitaxy (MOMBE law), are available in addition to the above. Moreover, the current diffusion layer is selectable to arbitration out of an AlxGa1-xAs (0.6< x<0.9) layer, zIn(AlyGa1-y)1-zP (0<=y<=1, 0<=z<=1), and a GaP layer, and may be formed by the monolayer, or may be formed in the combination of two or more layers.

[0032] Next, the sulfuric acid as shown in drawing 2 (b), after carrying out the polish of the front face of the non dope mold GaAs substrate 10: Process by the etchant of a hydrogen-peroxide system. Moreover, the n mold GaP substrate 1 is similarly processed by sulfuric-acid:hydrogen-peroxide system etchant. After fully pure-water-washing and drying each substrate, front faces are stuck and it processes in 1-hour hydrogen at 800 degrees C. By carrying out like this, the n mold GaP substrate 1 is joined to the n mold GaP cap layer 2 on the non dope mold GaAs substrate 10.

[0033] Furthermore, as shown in drawing 2 (c), etching clearance of the non dope mold GaAs substrate 10 and the p mold GaAs buffer layer 11 is carried out by ammonia:hydrogen-peroxide system etchant. The ratio of the ammonia/hydrogen peroxide at this time chooses as arbitration the ratio which both the non dope mold GaAs substrate 10 and the p mold GaAs buffer layer 11 can etch selectively to the aluminum0.68Ga0.32As current diffusion layer 7. A sulfuric acid removes the oxide film of aluminum0.68Ga0.32As current diffusion layer 7 front face after that.

[0034] Finally, thickness of the n mold GaP substrate 1 is made into predetermined thickness, p mold electrode (100micrometerphi: not shown) of a circle configuration is formed by AuZn/Mo/Au on the p mold aluminum0.68Ga0.32As current diffusion layer 7, four n mold electrodes (50micrometerphi: not shown) of a circle configuration are formed by AuSi on the n mold GaP substrate 1, and a semi-conductor light emitting device is obtained.

[0035] Thus, the thing whose external quantum efficiency in the bare-chip (bare chip) at the time of using an opaque substrate to luminescence wavelength was about 3 - 4% the obtained semi-conductor light emitting device In the semi-conductor light emitting device using the gestalt of the 1st operation, since the light which goes in the direction of an n mold GaP substrate, the light by which total reflection was carried out on the chip front face were taken out, the external quantum efficiency in a bare-chip improved 7 - 8%, and twice [about].

[0036] Moreover, although the external quantum efficiency of a semi-conductor light emitting device when a GaAs substrate and a GaP substrate manufacture using both the substrates of p mold falls rather than the thing of structure which used 1 - 2%, and an optical absorption substrate With the gestalt of operation of **** 1, since the non dope mold GaAs substrate 10 and the n mold GaP substrate 1 are used The decline in the luminous efficiency by the diffusion to the luminous layer of p mold dopant hot [at the time of the epitaxial growth of two or more semi-conductor layers and junction of the n mold GaP cap layer 2 on the non dope mold GaAs substrate 10 and the n mold GaP substrate 1] is suppressed by the minimum, and external quantum efficiency improves. Therefore, it understands it that the effectiveness which controls diffusion of a dopant is large enough to use the non dope mold GaAs substrate 10 and the n mold GaP substrate 1.

[0037] Moreover, according to the manufacture approach of the above-mentioned semi-conductor light emitting device, cost lowering of the semi-conductor light emitting device manufactured to the p mold GaP substrates of 2 inch phi being the prices of tens of thousands of yen/sheet since the n mold GaP substrate 1 was reasonable in thousands of yen/[a sheet and] is also realizable.

[0038] (Gestalt of the 2nd operation) Drawing 3 (a) thru/or (c) are drawings showing the semi-conductor light emitting device formed in the gestalt of operation of the 2nd of this invention, and drawing 3 (a) is [a plan and drawing 3 (c) of a side elevation and drawing 3 (b)] bottom views.

[0039] The structure of the semi-conductor light emitting device 200 formed in the gestalt of the 2nd operation For example, on the n mold GaP growth phase 31 The n mold GaP cap layer 32, n mold 0.77In0.23P interlayer 33, (aluminum0.2Ga0.8) The n mold aluminum0.5In0.5P cladding layer 34, p mold (aluminum0.3Ga0.7) The laminating of 0.5In0.5P barrier layer 35, the p mold aluminum0.5In0.5P cladding layer 36, the p mold aluminum0.7Ga0.3As current diffusion layer 37, and two or more semi-conductor layers of p mold (aluminum0.5Ga0.5) 0.5In0.5P protective layer 38 grade is carried out one by one. And p mold electrode 39 of the circle configuration which consists of AuBe/Mo/Au, and four n mold electrodes 40 of a circle configuration which consist of AuSi(s) are formed in the vertical side of the semi-conductor light emitting device 200.

[0040] Next, the manufacture approach of the semi-conductor light emitting device in the gestalt of the 2nd operation is explained to a detail.

[0041] Drawing 4 (a) thru/or (c) are process drawings showing the manufacture approach of a semi-conductor light emitting device of having used the gestalt of operation of the 2nd of this invention.

[0042] As shown in drawing 4 (a), on the n mold GaAs substrate 41 The p mold GaAs buffer layer 42 (1 micrometer), p mold (aluminum0.5Ga0.5) 0.5In0.5P protective layer 38 (0.1 micrometers), The p mold aluminum0.7Ga0.3As current diffusion layer 37 (5 micrometers), the p mold aluminum0.5In0.5P cladding layer 36 (1 micrometer), p mold (aluminum0.3Ga0.7) 0.5In0.5P barrier layer 35 (0.5 micrometers), Sequential growth of the n mold aluminum0.5In0.5P cladding layer 34 (1 micrometer), n mold (aluminum0.2Ga0.8) 0.77In0.23P interlayer 33 (0.15 micrometers), the n mold GaP cap layer 32 (1 micrometer), etc. is carried out for example, by the organic metal chemical-vapor-deposition method (MOCVD law). Moreover, as a p mold dopant, Zn, Mg, etc. are used, for example. In addition, as the growth approach, various approaches, such as molecular beam epitaxy (MBE law) and organic metal molecular beam epitaxy (MOMBE law), are available in addition to the above. Moreover, the protective layer is selectable to arbitration, and may form an ingredient with few aluminum contents than the current diffusion layer out of zIn(AlyGa1-y)1-zP (0<=y<=1, 0<=z<=1), a GaP layer, etc. by the monolayer, or may form it in the combination of two or more layers.

[0043] Next, as shown in drawing 4 (b), epitaxial growth of the n mold GaP growth phase 31 is carried out to the thickness of 100-150 micrometers by liquid phase epitaxy (LPE law). In addition, as the growth approach, various approaches, such as a vapor-phase-epitaxial-growth method (VPE law) and an organic metal chemical-vapor-deposition method (MOCVD law), are available in addition to the above.

[0044] Furthermore, as shown in drawing 4 (c), the n mold GaAs substrate 41 and the p mold GaAs buffer layer 42 are etched by ammonia:hydrogen-peroxide system etchant. The ratio of the ammonia/hydrogen peroxide at this time chooses as arbitration the ratio which the n mold GaAs substrate 41 and the p mold GaAs buffer layer 42 can etch selectively to p mold (aluminum0.5Ga0.5) 0.5In0.5P protective layer 38.

[0045] Finally, p mold electrode (100micrometerphi: not shown) of a circle configuration is formed by AuBe/Mo/Au on p mold (aluminum0.5Ga0.5) 0.5In0.5P protective layer 38, four n mold electrodes (50micrometerphi: not shown) of the circle configuration of 50 micrometerphi are formed by AuSi on the n mold GaP growth phase 31, and a semi-conductor light emitting device is obtained.

[0046] Thus, since the obtained semi-conductor light emitting device took out the light from which that whose external quantum efficiency in the bare-chip at the time of using an opaque substrate to luminescence wavelength was about 1 - 1.5% goes in the n mold GaP growth phase 31 direction in the semi-conductor light emitting device using the gestalt of the 2nd operation, the light by which total reflection was carried out on the chip front face, its external quantum efficiency in a bare-chip improved 2 - 3%, and twice [about].

[0047] Moreover, since the n mold GaAs substrate 41 is used unlike the case of the gestalt of the 1st operation and diffusion of p mold dopant to the inside of the n mold GaAs substrate 41 from the p mold GaAs buffer layer 42 hot [at the time of epitaxial growth], p mold (aluminum0.5Ga0.5) 0.5In0.5P protective layer 38, and the p mold aluminum0.7Ga0.3As current diffusion layer 37 is controlled, resistivity is maintained low. Therefore, since the acceptor concentration of the front face of p mold (aluminum0.5Ga0.5) 0.5In0.5P protective layer 38 which forms p mold electrode can be kept high and ohmic contact is obtained easily, compared with the former, lowering of the operating voltage of 0.05-0.1V is realizable. Furthermore, since the polish process on the front face of a wafer is unnecessary, simplification of a process is possible.

[0048] Moreover, to the GaAs substrates of the non dope mold of 2 inch phi being the prices of 10,000 - 20,000 yen/sheet, the GaAs substrate 41 of n mold is thousands of yen/sheet, and even if compared with the gestalt of the 1st operation, cost lowering of the further semi-conductor light emitting device is realizable according to the manufacture approach of the above-mentioned semi-conductor light emitting device.

[0049] Moreover, although aluminum mixed-crystal ratio of the p mold aluminum0.7Ga0.3As current diffusion layer 37 is highly set about to 0.70 with the gestalt of operation of **** 2 in order to lessen the absorption of light more, the front face can be equipped with p mold (aluminum0.5Ga0.5) 0.5In0.5P protective layer 38 for antioxidizing of this layer. Since there are few contents of aluminum than the p mold aluminum0.7Ga0.3As current diffusion layer 37, this p mold (aluminum0.5Ga0.5) 0.5In0.5P protective layer 38 has the description that the moisture resistance of a semi-conductor light emitting device improves. Although there were some which deteriorated to 70% of initial luminous intensity in 1000 hours with structure without p mold (aluminum0.5Ga0.5) 0.5In0.5P protective layer 38 by the elevated temperature and the energization trial (50mA) under highly humid (85 degrees C, 90%) On these conditions, what has large degradation is to 90% of initial luminous intensity, and, as for the semi-conductor light emitting device of this example, it is shown, as for luminous-intensity degradation in 1000 hours that p mold (aluminum0.5Ga0.5) 0.5In0.5P protective layer 38 is functioning effectively.

[0050]

[Effect of the Invention] The process which carries out the laminating of the p type semiconductor layer which consists of a monolayer or two or more layers on a non dope mold or an n mold GaAs substrate according to this invention, The process which carries out the laminating of the luminous layer which consists of a monolayer of the semiconductor material of an AlGaInP system, or two or more layers on a p type semiconductor layer, The process which carries out the laminating of the semi-conductor layer which consists of a monolayer of n mold, or two or more layers on a luminous layer, Since the transparence substrate mold semi-conductor light emitting device is produced without having the process which forms an n mold GaP thick-film layer, and the process which removes a non dope mold or an n mold GaAs substrate, and using p mold substrate and a thick-film layer on a n-type-semiconductor layer It becomes possible to control the diffusion to the barrier layer of p mold dopant at the time of high temperature processing, to maintain high internal quantum efficiency, and to obtain the semi-conductor light emitting device of high brightness. Furthermore, since diffusion of p mold dopant to the GaAs substrate from the p type semiconductor layer which grows epitaxially on an n mold GaAs substrate is controlled when a GaAs substrate is n mold, the ohmic contact of p mold electrode is easy to be obtained, and since the resistivity of a p type semiconductor layer is also maintained low, it becomes possible to obtain a semi-conductor light emitting device with more low operating voltage.

[0051] Therefore, although the external quantum efficiency of a semi-conductor light emitting device when a GaAs substrate and a GaP substrate manufacture using both p mold substrates falls rather than the thing of structure which used the optical absorption substrate When using a non dope mold GaAs substrate and an n mold GaP substrate The decline in the luminous efficiency by the diffusion to the luminous layer of p mold dopant hot [at the time of the epitaxial growth of two or more semi-conductor layers and junction of the n mold GaP cap layer on a GaAs substrate and an n mold GaP substrate] is suppressed by the minimum, and external quantum efficiency improves. Therefore, the effectiveness which controls the diffusion of a dopant in the case of using a non dope mold GaAs substrate and an n mold GaP substrate is large enough. Moreover, since diffusion of p mold dopant from a p type semiconductor layer hot [at the time of epitaxial growth] to the inside of an n mold GaAs substrate is controlled when using an n mold GaAs substrate, resistivity is maintained low. Therefore, since the acceptor concentration of the p type semiconductor layer front face of the part which forms p mold electrode can be kept high and ohmic contact is obtained easily, compared with the former, lowering of operating voltage is realizable.

[0052] Moreover, the stroke to which the stroke which forms an n mold GaP thick-film layer arranges an n mold GaP substrate on a n-type-semiconductor layer, Since it has the stroke which joins an n mold GaP substrate to a n-type-semiconductor layer top face by high temperature processing and junction formation of the n mold GaP substrate is carried out by high temperature processing on the n-type-semiconductor layer top face An n mold GaP substrate thick enough can be produced easily, and it becomes possible to prevent lowering of the processing yield by the wafer crack.

[0053] Therefore, since an n mold GaP substrate with a cheap price can be used compared with the case where junction formation of the conventional p mold GaP substrate is carried out, in accordance with improvement in a product yield, a manufacturing cost can decrease substantially.

[0054] Moreover, since a production process can be further simplified compared with the approach of adjusting a semi-conductor substrate since the n mold GaP thick-film layer is formed with epitaxial growth on a n-type-semiconductor layer, it becomes possible to manufacture a semi-conductor light emitting device more efficiently.

[0055] A manufacturing cost can decrease substantially -- follow, for example, use neither the abbreviation of the polish process on the front face of a wafer, nor an n mold GaP substrate, but it uses only the GaAs substrate of n mold with a cheap price.

[0056] Moreover, the p type semiconductor layer which consists of a monolayer which carries out a laminating on a non dope mold or an n mold GaAs substrate, or two or more layers It has a transparent current diffusion layer to the luminescence wavelength of the light from a luminous layer at least. Furthermore, since the current diffusion layer is formed of the monolayer chosen from an AlxGa1-xAs (0.6< x<0.9) layer, zIn(AlyGa1-y)1-zP (0<=y<=1, 0<=z<=1), and a GaP layer, or two or more layers It becomes possible to decrease the light which it becomes easy to diffuse the current from p mold electrode, and is absorbed by p mold electrode.

[0057] Therefore, since a current can be poured into the whole luminous layer, the external outgoing radiation effectiveness of the light from a luminous layer improves. Furthermore, it enables zIn(AlyGa1-y)1-zP (0<=y<=1, 0<=z<=1) and a GaP layer to improve moisture resistance, since there are few aluminum contents compared with an AlxGa1-xAs (0.6< x<0.9) layer.

[0058] Moreover, since the AlxGa1-xAs (0.6< x<0.9) layer is formed at least (AlyGa1-y) on a non dope mold or an n mold GaAs substrate after forming a zIn1-zP (0<=y<=1, 0<=z<=1) layer or a GaP layer, it becomes possible to improve moisture resistance.

[0059] Therefore, luminous-intensity degradation of an elevated temperature and the semi-conductor light emitting device under highly humid becomes small, and dependability improves.

[Translation done.]

* NOTICES *

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1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] (a) Or (c) is the side elevation, plan, and bottom view of the semi-conductor light emitting device formed in the gestalt of operation of the 1st of this invention.
[Drawing 2] (a) Or (c) is process drawing showing the manufacture approach of the semi-conductor light emitting device by the gestalt of operation of the 1st of this invention.
[Drawing 3] (a) Or (c) is the side elevation, plan, and bottom view of the semi-conductor light emitting device formed in the gestalt of operation of the 2nd of this invention.
[Drawing 4] (a) Or (c) is process drawing showing the manufacture approach of the semi-conductor light emitting device by the gestalt of operation of the 2nd of this invention.
[Drawing 5] (a) Or (b) is process drawing showing the manufacture approach of the semi-conductor light emitting device by the conventional example.
[Drawing 6] (a) Or (c) is process drawing showing the manufacture approach of the semi-conductor light emitting device by other conventional examples.
[Description of Notations]
1 N Mold GaP Substrate
2 32 n mold GaP cap layer
3 33 n mold (aluminum0.2Ga0.8) 0.77In0.23P interlayer
4 34 n mold aluminum0.5In0.5P cladding layer
5 P Mold Ga0.5In0.5P Barrier Layer
6 36 p mold aluminum0.5In0.5P cladding layer
7 P Mold Aluminum0.68Ga0.32As Current Diffusion Layer
10 Non Dope Mold GaAs Substrate
11 42 p mold GaAs buffer layer
31 N Mold GaP Growth Phase
35 P Mold (Aluminum0.3Ga0.7) 0.5In0.5P Barrier Layer
37 P Mold Aluminum0.7Ga0.3As Current Diffusion Layer
38 P Mold (Aluminum0.5Ga0.5) 0.5In0.5P Protective Layer
41 N Mold GaAs Substrate
100,200 Semi-conductor light emitting device

[Translation done.]

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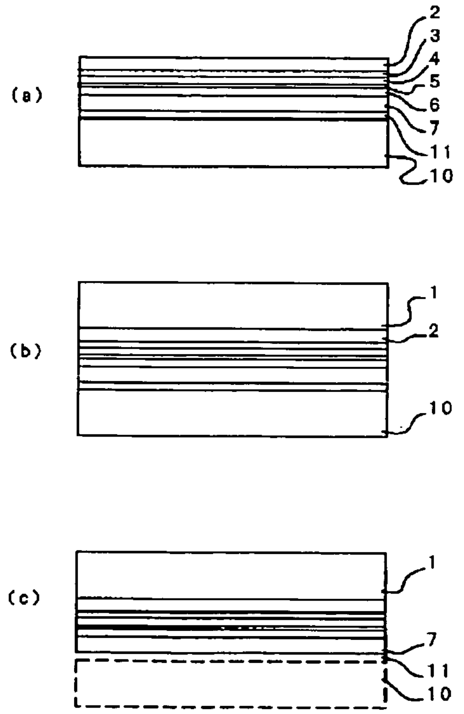
最終頁に続く

(54)【発明の名称】　半導体発光素子の製造方法

(57)【要約】

【課題】　半導体発光素子製造時の活性層へのドーパントの拡散を防止する。

【解決手段】　ノンドープ型ＧａＡｓ基板１０上に単層あるいは複数層からなるｐ型半導体層、ＡｌＧａＩｎＰ系の半導体材料の発光層、ｎ型半導体層を順次形成後、ｎ型ＧａＰ厚膜層１を形成する工程と、ノンドープ型ＧａＡｓ基板１０を除去する工程とを有することを特徴とする。



【特許請求の範囲】

【請求項１】　基板上に半導体層が積層形成されてなる半導体発光素子の製造方法において、
ノンドープ型ＧａＡｓ基板上に単層あるいは複数層からなるｐ型半導体層を積層する工程と、
前記ｐ型半導体層上にＡｌＧａＩｎＰ系の半導体材料の単層あるいは複数層からなる発光層を積層する工程と、
前記発光層上にｎ型の単層あるいは複数層からなる半導体層を積層する工程と、
前記ｎ型半導体層上にｎ型ＧａＰ厚膜層を形成する工程と、
前記ノンドープ型ＧａＡｓ基板を除去する工程と、
を有することを特徴とする半導体発光素子の製造方法。

【請求項２】　基板上に半導体層が積層形成されてなる半導体発光素子の製造方法において、
ｎ型ＧａＡｓ基板上に単層あるいは複数層からなるｐ型半導体層を積層する工程と、
前記ｐ型半導体層上にＡｌＧａＩｎＰ系の半導体材料の単層あるいは複数層からなる発光層を積層する工程と、
前記発光層上にｎ型の単層あるいは複数層からなる半導体層を積層する工程と、
前記ｎ型半導体層上にｎ型ＧａＰ厚膜層を形成する工程と、
前記ｎ型ＧａＡｓ基板を除去する工程と、
を有することを特徴とする半導体発光素子の製造方法。

【請求項３】　前記ｎ型ＧａＰ厚膜層を形成する行程は、
前記ｎ型半導体層上にｎ型ＧａＰ基板を配設する行程と、
前記ｎ型ＧａＰ基板を高温処理により前記ｎ型半導体層上面に接合する行程と、
を含むことを特徴とする請求項１又は２に記載の半導体発光素子の製造方法。

【請求項４】　前記ｎ型ＧａＰ厚膜層を形成する行程は、
前記ｎ型半導体層上にｎ型ＧａＰ成長層をエピタキシャル成長する行程を含むことを特徴とする請求項１又は２に記載の半導体発光素子の製造方法。

【請求項５】　前記ノンドープ型又は前記ｎ型ＧａＡｓ基板上に積層する単層あるいは複数層からなる前記ｐ型半導体層は、
少なくとも前記発光層からの光の発光波長に対して透明な電流拡散層を含むことを特徴とする請求項１乃至４に記載の半導体発光素子の製造方法。

【請求項６】　前記電流拡散層は、
$\mathrm{Al_xGa_{1-x}As}$（０．６＜ｘ＜０．９）層、$(\mathrm{Al_yGa_{1-y}})_z\mathrm{In_{1-z}P}$（０≦ｙ≦１、０≦ｚ≦１）、ＧａＰ層の中から選ばれた単層あるいは複数層からなることを特徴とする請求項５に記載の半導体発光素子の製造方法。

【請求項７】　前記電流拡散層は、
前記ノンドープ型又は前記ｎ型ＧａＡｓ基板上に少なくとも前記$(\mathrm{Al_yGa_{1-y}})_z\mathrm{In_{1-z}P}$（０≦ｙ≦１、０≦ｚ≦１）層又は前記ＧａＰ層を形成後に前記$\mathrm{Al_xGa_{1-x}As}$（０．６＜ｘ＜０．９）層を形成することを特徴とする請求項６に記載の半導体発光素子の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、半導体発光素子の製造方法に関し、特に、高輝度の半導体発光素子の製造方法に関する。

【０００２】

【従来の技術】近年、光通信や情報表示パネル等に半導体発光素子が広く用いられている。これらの半導体発光素子は、高輝度であることが重要である。半導体発光素子の輝度すなわち効率は、内部量子効率と外部出射効率によって決まり、このうち外部出射効率は、素子構造に大きく影響される。

【０００３】半導体発光素子では、発光波長に対して透明な基板を用いることが外部出射効率を向上させることを目的として一般に行われている。これは、発光波長に対して不透明な基板を用いた場合に、半導体発光素子の上面への出射光しか利用できないのに対し、発光波長に対して透明な基板を用いた場合には、上面だけでなく４つの側面からも光を取り出すことができるからである。また、半導体発光素子の下面における反射光も、発光波長に対して透明な基板を用いた場合には、上面及び側面から出射させることが可能となる。

【０００４】この発光波長に対して透明な基板を用いる製造方法は、ＩｎＧａＡｓＰ系の半導体材料を用いた赤外半導体発光素子、ＡｌＧａＡｓ系の半導体材料を用いた赤色又は赤外半導体発光素子、ＧａＡｓＰ系の半導体材料を用いた黄色半導体発光素子、ＧａＰ系の半導体材料を用いた緑色半導体発光素子等に適用されている。

【０００５】一方、ＡｌＧａＩｎＰ系の半導体発光素子においては、発光波長に対して透明な基板を用いる製造方法として、例えば特開平６－２９６０４０号公報に開示されているようなものが知られている。この従来の半導体発光素子の製造方法は、図５（ａ）又は（ｂ）に示すように、発光波長に対して不透明なＧａＡｓ基板５１上に発光層５３を含む複数の半導体層５５をエピタキシャル成長し、この上に発光波長に対して透明なＧａＰ基板５８を配設後熱処理を施すことによって上面に発光層５３を含む複数の半導体層５５をエピタキシャル成長形成したＧａＡｓ基板５１とＧａＰ基板５８とをウエハー接合し、更に発光波長に対して不透明なＧａＡｓ基板５１を除去して半導体発光素子を得る。

【０００６】また、ＡｌＧａＩｎＰ系の半導体発光素子での他の製造方法として、例えば特開平６－３０２８５

７号公報に開示されているようなものが知られている。この他の従来の半導体発光素子の製造方法は、図６（ａ）乃至（ｃ）に示すように、発光波長に対して不透明なＧａＡｓ基板６１上に発光層６３を含む複数の半導体層６５をエピタキシャル成長し、その後ＧａＰ電流拡散層６６を数１０μm成長し、発光波長に対して不透明なＧａＡｓ基板６１を除去し、除去した面にＧａＰ基板６８を配設後熱処理を施すことによってウエハー接合して半導体発光素子を得る。この場合、発光層上に成長するＧａＰ電流拡散層６６は、成長時間とＧａＡｓ基板６１を除去した後のエピタキシャル成長層６７の機械的強度との兼ね合いで、一般に５０～１００μm程度である。これは、５０μm以下であるとＧａＡｓ基板６１を除去した後のエピタキシャル成長層６７を取り扱う時に割れやすく、１００μm以上であると成長時間が長くなり半導体発光素子のコストが高くなるからである。

【０００７】

【発明が解決しようとする課題】上記従来の半導体発光素子の製造方法においては、下記に示すようなような問題点があった。

【０００８】（１）発光波長に対して不透明なＧａＡｓ基板上に発光層をエピタキシャル成長し、この上に発光波長に対して透明なＧａＰ基板を配設後熱処理を施すことによって上面にエピタキシャル成長層を形成したＧａＡｓ基板とＧａＰ基板とをウエハー接合し、更に発光波長に対して不透明なＧａＡｓ基板を除去するという製造方法の場合は、発光波長に対して不透明なＧａＡｓ基板か、発光波長に対して透明なＧａＰ基板のうち、いずれか一方をｐ型基板にする必要がある。

【０００９】ところが、ｐ型基板は、通常抵抗率を低くするためｐ型ドーパント（例えば、Ｚｎ、Ｍｇ等）を$1\times10^{19}\mathrm{cm}^{-3}$程度ドーピングしなければならず、ｐ型ドーパントの拡散係数が大きいこともあり、エピタキシャル成長あるいは、ウエハー接合の高温処理時に発光層にドーパントが拡散し、内部量子効率の低下が生じ、半導体発光素子の輝度が低下するという問題点があった。

【００１０】（２）発光波長に対して不透明なＧａＡｓ基板上に発光層をエピタキシャル成長し、その後ＧａＰ電流拡散層を数１０μm成長し、発光波長に対して不透明なＧａＡｓ基板を除去し、除去した面にＧａＰ基板を配設後熱処理を施すことによってウエハー接合するという製造方法では、ＧａＡｓ基板を除去してからＧａＰ基板を接合するまでの間、数１０μmのかなり薄い基板を取り扱う必要があり、ウエハー割れにより、量産時には歩留りが低下するという問題点があった。

【００１１】（３）また、上記（２）の問題点に加えて、ＧａＡｓ基板にｎ型を用いた場合、数１０μmのＧａＰ電流拡散層はｐ型であるので、数μmの電流拡散層を形成する場合よりもドーパントの総量は多くなり、結果的に発光層へドーパントは拡散しやすくなるという問題点があった。

【００１２】（４）一方、上記（２）の問題点に加えて、ＧａＡｓ基板にｐ型を用いた場合、ｐ型ＧａＡｓ基板のドーパント量はｎ型ＧａＡｓ基板に比べて多いので、ドーパント拡散が更に多くなる。その結果、発光効率の低下が生じてしまい、光吸収基板を透明基板に置き換える効果は小さくなるという問題点があった。

【００１３】本発明の目的は、活性層からの発光をチップの上面に加えて側面からも取り出すことが可能で、且つ活性層へのドーパントの拡散を抑制することにり、高輝度の半導体発光素子を提供することにある。

【００１４】

【課題を解決するための手段】本発明は、上記問題点に鑑みなされたもので、半導体発光素子の製造方法において、請求項１に係わる発明の半導体発光素子は、基板上に半導体層が積層形成されてなる半導体発光素子の製造方法において、ノンドープ型ＧａＡｓ基板上に単層あるいは複数層からなるｐ型半導体層を積層する工程と、ｐ型半導体層上にＡｌＧａＩｎＰ系の半導体材料の単層あるいは複数層からなる発光層を積層する工程と、発光層上にｎ型の単層あるいは複数層からなる半導体層を積層する工程と、ｎ型半導体層上にｎ型ＧａＰ厚膜層を形成する工程と、ノンドープ型ＧａＡｓ基板を除去する工程とを有することを特徴としている。

【００１５】上記構成によれば、ｐ型基板を使用していないので、高温処理時のｐ型ドーパントの活性層への拡散が抑制され、高い内部量子効率が維持され高輝度の半導体発光素子を得ることが可能になる。

【００１６】また、請求項２に係わる発明の半導体発光素子は、基板上に半導体層が積層形成されてなる半導体発光素子の製造方法において、ｎ型ＧａＡｓ基板上に単層あるいは複数層からなるｐ型半導体層を積層する工程と、ｐ型半導体層上にＡｌＧａＩｎＰ系の半導体材料の単層あるいは複数層からなる発光層を積層する工程と、発光層上にｎ型の単層あるいは複数層からなる半導体層を積層する工程と、ｎ型半導体層上にｎ型ＧａＰ厚膜層を形成する工程と、ｎ型ＧａＡｓ基板を除去する工程とを有することを特徴としている。

【００１７】上記構成によれば、ｐ型基板を使用していないので、高温処理時のｐ型ドーパントの活性層への拡散が抑制され、高い内部量子効率が維持され高輝度の半導体発光素子を得ることが可能になる。更に、ＧａＡｓ基板がｎ型であるので、ｎ型ＧａＡｓ基板上にエピタキシャル成長するｐ型半導体層からのＧａＡｓ基板へのｐ型ドーパントの拡散が抑制されるので、ｐ型電極のオーミックコンタクトが得られ易く、ｐ型半導体層の抵抗率も低く維持されるので、より動作電圧の低い半導体発光素子を得ることが可能になる。

【００１８】また、請求項３に係わる発明は、請求項１又は２に係わる半導体発光素子の製造方法において、ｎ

型ＧａＰ厚膜層を形成する行程が、ｎ型半導体層上にｎ型ＧａＰ基板を配設する行程と、ｎ型ＧａＰ基板を高温処理によりｎ型半導体層上面に接合する行程とを含むことを特徴としている。

【００１９】上記構成によれば、ｎ型ＧａＰ基板を高温処理によりｎ型半導体層上面に接合形成しているので、十分に厚いｎ型ＧａＰ基板を容易に作製することができ、ウエハー割れによる処理歩留の低下を防ぐことが可能になる。

【００２０】また、請求項４に係わる発明は、請求項１又は２に係わる半導体発光素子の製造方法において、ｎ型ＧａＰ厚膜層を形成する行程が、ｎ型半導体層上にｎ型ＧａＰ成長層をエピタキシャル成長する行程を含むことを特徴としている。

【００２１】上記構成によれば、ｎ型半導体層上にｎ型ＧａＰ厚膜層をエピタキシャル成長で形成しているので、請求項３に比べて製造工程を簡略化することができるので、より効率良く半導体発光素子を製造することが可能になる。

【００２２】また、請求項５又は６に係わる発明は、請求項１乃至４に係わる半導体発光素子の製造方法において、ノンドープ型又はｎ型ＧａＡｓ基板上に積層する単層あるいは複数層からなるｐ型半導体層が、少なくとも発光層からの光の発光波長に対して透明な電流拡散層を含むことを特徴とし、更に電流拡散層は$Al_xGa_{1-x}As$（$0.6<x<0.9$）層、$(Al_yGa_{1-y})_zIn_{1-z}P$（$0 \leqq y \leqq 1$、$0 \leqq z \leqq 1$）、ＧａＰ層の中から選ばれた単層あるいは複数層からなることを特徴としている。

【００２３】上記構成によれば、前記発光層からの光の発光波長に対して透明な電流拡散層を備えているので、ｐ型電極からの電流が拡散しやすくなり、ｐ型電極に吸収される光を減少させることが可能になる。更に、$(Al_yGa_{1-y})_zIn_{1-z}P$（$0 \leqq y \leqq 1$、$0 \leqq z \leqq 1$）、ＧａＰ層は$Al_xGa_{1-x}As$（$0.6<x<0.9$）層に比べてＡｌ含有量が少ないので耐湿性を向上することが可能になる。

【００２４】また、請求項７に係わる発明は、請求項６に係わる半導体発光素子の製造方法において、ノンドープ型又はｎ型ＧａＡｓ基板上に少なくとも$(Al_yGa_{1-y})_zIn_{1-z}P$（$0 \leqq y \leqq 1$、$0 \leqq z \leqq 1$）層又はＧａＰ層を形成後に$Al_xGa_{1-x}As$（$0.6<x<0.9$）層を形成することを特徴としている。

【００２５】上記構成によれば、活性層上に$Al_xGa_{1-x}As$（$0.6<x<0.9$）層、更にその外側に少なくとも$(Al_yGa_{1-y})_zIn_{1-z}P$（$0 \leqq y \leqq 1$、$0 \leqq z \leqq 1$）層、又はＧａＰ層を備えているので、$Al_xGa_{1-x}As$（$0.6<x<0.9$）層単層の場合に比べて耐湿性を向上することが可能になる。

【００２６】

【発明の実施の形態】以下、本発明の実施の形態を図面を参照して説明する。

【００２７】（第１の実施の形態）図１（ａ）乃至（ｃ）は本発明の第１の実施の形態において形成された半導体発光素子を示す図であり、図１（ａ）は側面図、図１（ｂ）は上面図、図１（ｃ）は底面図である。

【００２８】第１の実施の形態において形成された半導体発光素子１００の構造は、例えばｎ型ＧａＰ基板１上に、ｎ型ＧａＰキャップ層２、ｎ型$(Al_{0.2}Ga_{0.8})_{0.77}In_{0.23}P$中間層３、ｎ型$Al_{0.5}In_{0.5}P$クラッド層４、ｐ型$Ga_{0.5}In_{0.5}P$活性層５、ｐ型$Al_{0.5}In_{0.5}P$クラッド層６、ｐ型$Al_{0.68}Ga_{0.32}As$電流拡散層７等の複数の半導体層が順次積層されている。そして、半導体発光素子１００の上下面には、例えばＡｕＺｎ／Ｍｏ／Ａｕからなる円形状のｐ型電極８と、例えばＡｕＳｉからなる４個の円形状のｎ型電極９が形成されている。

【００２９】次に、第１の実施の形態における半導体発光素子の製造方法について詳細に説明する。

【００３０】図２（ａ）乃至（ｃ）は本発明の第１の実施の形態を用いた半導体発光素子の製造方法を示す工程図である。

【００３１】図２（ａ）に示すようにノンドープ型ＧａＡｓ基板１０上に、ｐ型ＧａＡｓバッファー層１１（１μｍ）、ｐ型$Al_{0.68}Ga_{0.32}As$電流拡散層７（５μｍ）、ｐ型$Al_{0.5}In_{0.5}P$クラッド層６（１μｍ）、ｐ型$Ga_{0.5}In_{0.5}P$活性層５（０．５μｍ）、ｎ型$Al_{0.5}In_{0.5}P$クラッド層４（１μｍ）、ｎ型$(Al_{0.2}Ga_{0.8})_{0.77}In_{0.23}P$中間層３（０．１５μｍ）、ｎ型ＧａＰキャップ層２（１μｍ）等を、例えば有機金属化学気相成長法（ＭＯＣＶＤ法）により順次成長する。又、ｐ型ドーパントとしては、例えば、Ｚｎ、Ｍｇ等が使用される。尚、成長方法としては、上記以外に分子線エピタキシャル成長法（ＭＢＥ法）、有機金属分子線エピタキシャル成長法（ＭＯＭＢＥ法）等色々な方法が利用可能である。又、電流拡散層は$Al_xGa_{1-x}As$（$0.6<x<0.9$）層、$(Al_yGa_{1-y})_zIn_{1-z}P$（$0 \leqq y \leqq 1$、$0 \leqq z \leqq 1$）、ＧａＰ層の中から任意に選択可能であり、単層で形成しても良いし、あるいは複数層の組合せで形成しても良い。

【００３２】次に、図２（ｂ）に示すように、ノンドープ型ＧａＡｓ基板１０の表面をポリッシュした後、硫酸：過酸化水素系のエッチャントで処理する。また、ｎ型ＧａＰ基板１を同様に硫酸：過酸化水素系エッチャントで処理する。各々の基板を十分に純水洗浄、乾燥した後、表面同士を密着させ８００℃で１時間水素中で処理する。こうすることにより、ノンドープ型ＧａＡｓ基板１０上のｎ型ＧａＰキャップ層２とｎ型ＧａＰ基板１が接合される。

【００３３】更に、図２（ｃ）に示すようにアンモニ

ア：過酸化水素系エッチャントによりノンドープ型ＧａＡｓ基板１０及びｐ型ＧａＡｓバッファー層１１をエッチング除去する。この時のアンモニア／過酸化水素の比率はノンドープ型ＧａＡｓ基板１０及びｐ型ＧａＡｓバッファー層１１の両方がＡｌ$_{0.68}$Ｇａ$_{0.32}$Ａｓ電流拡散層７に対して選択的にエッチングできる比率を任意に選ぶ。その後硫酸によりＡｌ$_{0.68}$Ｇａ$_{0.32}$Ａｓ電流拡散層７表面の酸化膜を除去する。

【００３４】最後に、ｎ型ＧａＰ基板１の厚さを所定の厚さにし、ｐ型Ａｌ$_{0.68}$Ｇａ$_{0.32}$Ａｓ電流拡散層７上に例えばＡｕＺｎ／Ｍｏ／Ａｕにより円形状のｐ型電極（１００μｍφ：図示せず）を形成し、ｎ型ＧａＰ基板１上に例えばＡｕＳｉにより４個の円形状のｎ型電極（５０μｍφ：図示せず）を形成して半導体発光素子を得る。

【００３５】このようにして得られた半導体発光素子は、発光波長に対し不透明な基板を用いた場合のｂａｒｅ－チップ（ベアーチップ）での外部量子効率が３～４％程度であったものが、第１の実施の形態を用いた半導体発光素子では、ｎ型ＧａＰ基板方向に向かう光やチップ表面で全反射された光等も取り出すことができるので、ｂａｒｅ－チップでの外部量子効率が７～８％と約２倍に向上した。

【００３６】また、ＧａＡｓ基板とＧａＰ基板とが共にｐ型の基板を使用して製造した場合の半導体発光素子の外部量子効率は、１～２％と光吸収基板を用いた構造のものよりも低下するが、本第１の実施の形態では、ノンドープ型ＧａＡｓ基板１０とｎ型ＧａＰ基板１を使用しているので、複数の半導体層のエピタキシャル成長時やノンドープ型ＧａＡｓ基板１０上のｎ型ＧａＰキャップ層２とｎ型ＧａＰ基板１の接合時の高温における、ｐ型ドーパントの発光層への拡散による発光効率の低下は最小限度に抑えられており、外部量子効率は向上する。従って、ノンドープ型ＧａＡｓ基板１０とｎ型ＧａＰ基板１とを使用することは、ドーパントの拡散を抑制する効果が十分大きいことがわかる。

【００３７】また、上記半導体発光素子の製造方法によると、２インチφのｐ型ＧａＰ基板が数万円／枚の価格であるのに対し、ｎ型ＧａＰ基板１は数千円／枚とリーズナブルであるので、製造した半導体発光素子のコスト低下を実現することもできる。

【００３８】（第２の実施の形態）図３（ａ）乃至（ｃ）は本発明の第２の実施の形態において形成された半導体発光素子を示す図であり、図３（ａ）は側面図、図３（ｂ）は上面図、図３（ｃ）は底面図である。

【００３９】第２の実施の形態において形成された半導体発光素子２００の構造は、例えばｎ型ＧａＰ成長層３１上に、ｎ型ＧａＰキャップ層３２、ｎ型（Ａｌ$_{0.2}$Ｇａ$_{0.8}$）$_{0.77}$Ｉｎ$_{0.23}$Ｐ中間層３３、ｎ型Ａｌ$_{0.5}$Ｉｎ$_{0.5}$Ｐクラッド層３４、ｐ型（Ａｌ$_{0.3}$Ｇａ$_{0.7}$）$_{0.5}$Ｉｎ$_{0.5}$Ｐ活性層３５、ｐ型Ａｌ$_{0.5}$Ｉｎ$_{0.5}$Ｐクラッド層３６、ｐ型Ａｌ$_{0.7}$Ｇａ$_{0.3}$Ａｓ電流拡散層３７、ｐ型（Ａｌ$_{0.5}$Ｇａ$_{0.5}$）$_{0.5}$Ｉｎ$_{0.5}$Ｐ保護層３８等の複数の半導体層が順次積層されている。そして、半導体発光素子２００の上下面には、例えばＡｕＢｅ／Ｍｏ／Ａｕからなる円形状のｐ型電極３９と、例えばＡｕＳｉからなる４個の円形状のｎ型電極４０が形成されている。

【００４０】次に、第２の実施の形態における半導体発光素子の製造方法について詳細に説明する。

【００４１】図４（ａ）乃至（ｃ）は本発明の第２の実施の形態を用いた半導体発光素子の製造方法を示す工程図である。

【００４２】図４（ａ）に示すようにｎ型ＧａＡｓ基板４１上に、ｐ型ＧａＡｓバッファー層４２（１μｍ）、ｐ型（Ａｌ$_{0.5}$Ｇａ$_{0.5}$）$_{0.5}$Ｉｎ$_{0.5}$Ｐ保護層３８（０．１μｍ）、ｐ型Ａｌ$_{0.7}$Ｇａ$_{0.3}$Ａｓ電流拡散層３７（５μｍ）、ｐ型Ａｌ$_{0.5}$Ｉｎ$_{0.5}$Ｐクラッド層３６（１μｍ）、ｐ型（Ａｌ$_{0.3}$Ｇａ$_{0.7}$）$_{0.5}$Ｉｎ$_{0.5}$Ｐ活性層３５（０．５μｍ）、ｎ型Ａｌ$_{0.5}$Ｉｎ$_{0.5}$Ｐクラッド層３４（１μｍ）、ｎ型（Ａｌ$_{0.2}$Ｇａ$_{0.8}$）$_{0.77}$Ｉｎ$_{0.23}$Ｐ中間層３３（０．１５μｍ）、ｎ型ＧａＰキャップ層３２（１μｍ）等を、例えば有機金属化学気相成長法（ＭＯＣＶＤ法）により順次成長する。又、ｐ型ドーパントとしては、例えば、Ｚｎ、Ｍｇ等が使用される。尚、成長方法としては、上記以外に分子線エピタキシャル成長法（ＭＢＥ法）、有機金属分子線エピタキシャル成長法（ＭＯＭＢＥ法）等色々な方法が利用可能である。又、保護層は（Ａｌ$_{y}$Ｇａ$_{1-y}$）$_{z}$Ｉｎ$_{1-z}$Ｐ（$0 \leqq y \leqq 1$、$0 \leqq z \leqq 1$）、ＧａＰ層等の中から電流拡散層よりもＡｌ含有量の少ない材料を任意に選択可能であり、単層で形成しても良いし、あるいは複数層の組合せで形成しても良い。

【００４３】次に、図４（ｂ）に示すように、例えば液相エピタキシャル成長法（ＬＰＥ法）によりｎ型ＧａＰ成長層３１を１００～１５０μｍの厚さまでエピタキシャル成長させる。尚、成長方法としては、上記以外に気相エピタキシャル成長法（ＶＰＥ法）、有機金属化学気相成長法（ＭＯＣＶＤ法）等色々な方法が利用可能である。

【００４４】更に、図４（ｃ）に示すように、アンモニア：過酸化水素系エッチャントによりｎ型ＧａＡｓ基板４１及びｐ型ＧａＡｓバッファー層４２をエッチングする。この時のアンモニア／過酸化水素の比率はｎ型ＧａＡｓ基板４１及びｐ型ＧａＡｓバッファー層４２がｐ型（Ａｌ$_{0.5}$Ｇａ$_{0.5}$）$_{0.5}$Ｉｎ$_{0.5}$Ｐ保護層３８に対して選択的にエッチングできる比率を任意に選ぶ。

【００４５】最後に、ｐ型（Ａｌ$_{0.5}$Ｇａ$_{0.5}$）$_{0.5}$Ｉｎ$_{0.5}$Ｐ保護層３８上に例えばＡｕＢｅ／Ｍｏ／Ａｕにより円形状のｐ型電極（１００μｍφ：図示せず）を形成し、ｎ型ＧａＰ成長層３１上に例えばＡｕＳｉにより４

個の５０μｍφの円形状のｎ型電極（５０μｍφ：図示せず）を形成して半導体発光素子を得る。

【００４６】このようにして得られた半導体発光素子は、発光波長に対し不透明な基板を用いた場合のｂａｒｅ－チップでの外部量子効率が１～１．５％程度であったものが、第２の実施の形態を用いた半導体発光素子では、ｎ型ＧａＰ成長層３１方向に向かう光やチップ表面で全反射された光等も取り出すことができるので、ｂａｒｅ－チップでの外部量子効率が２～３％と約２倍に向上した。

【００４７】また、第１の実施の形態の場合と異なり、ｎ型ＧａＡｓ基板４１を使用しているので、エピタキシャル成長時の高温におけるｐ型ＧａＡｓバッファー層４２、ｐ型$(\mathrm{Al}_{0.5}\mathrm{Ga}_{0.5})_{0.5}\mathrm{In}_{0.5}\mathrm{P}$保護層３８、ｐ型$\mathrm{Al}_{0.7}\mathrm{Ga}_{0.3}\mathrm{As}$電流拡散層３７からのｎ型ＧａＡｓ基板４１中へのｐ型ドーパントの拡散が抑制されるので、抵抗率が低く維持される。従って、ｐ型電極を形成するｐ型$(\mathrm{Al}_{0.5}\mathrm{Ga}_{0.5})_{0.5}\mathrm{In}_{0.5}\mathrm{P}$保護層３８の表面のアクセプタ濃度を高く保つことができ、容易にオーミックコンタクトが得られるので、従来に比べ０．０５～０．１Ｖの動作電圧の低下が実現できる。更にウエハー表面のポリッシュ工程が不要であるので、工程の簡略化が可能である。

【００４８】また、上記半導体発光素子の製造方法によると、２インチφのノンドープ型のＧａＡｓ基板が１～２万円／枚の価格であるのに対し、ｎ型のＧａＡｓ基板４１は数千円／枚であり、第１の実施の形態に比べても更なる半導体発光素子のコスト低下を実現することができる。

【００４９】また、本第２の実施の形態では光の吸収をより少なくするために、ｐ型$\mathrm{Al}_{0.7}\mathrm{Ga}_{0.3}\mathrm{As}$電流拡散層３７のＡｌ混晶比を０．７０程度に高く設定しているが、この層の酸化防止のためにｐ型$(\mathrm{Al}_{0.5}\mathrm{Ga}_{0.5})_{0.5}\mathrm{In}_{0.5}\mathrm{P}$保護層３８を表面に備えていえる。このｐ型$(\mathrm{Al}_{0.5}\mathrm{Ga}_{0.5})_{0.5}\mathrm{In}_{0.5}\mathrm{P}$保護層３８は、ｐ型$\mathrm{Al}_{0.7}\mathrm{Ga}_{0.3}\mathrm{As}$電流拡散層３７よりもＡｌの含有量が少ないので、半導体発光素子の耐湿性が向上するという特徴がある。高温、高湿（８５℃、９０％）下での通電試験（５０ｍＡ）では、ｐ型$(\mathrm{Al}_{0.5}\mathrm{Ga}_{0.5})_{0.5}\mathrm{In}_{0.5}\mathrm{P}$保護層３８のない構造では１０００時間で初期光度の７０％まで劣化したものがあったが、同条件で本実施例の半導体発光素子は、１０００時間での光度劣化は劣化の大きいものでも初期光度の９０％までであり、ｐ型$(\mathrm{Al}_{0.5}\mathrm{Ga}_{0.5})_{0.5}\mathrm{In}_{0.5}\mathrm{P}$保護層３８が有効に機能していることが示されている。

【００５０】

【発明の効果】本発明によれば、ノンドープ型又はｎ型ＧａＡｓ基板上に単層あるいは複数層からなるｐ型半導体層を積層する工程と、ｐ型半導体層上にＡｌＧａＩｎＰ系の半導体材料の単層あるいは複数層からなる発光層を積層する工程と、発光層上にｎ型の単層あるいは複数層からなる半導体層を積層する工程と、ｎ型半導体層上にｎ型ＧａＰ厚膜層を形成する工程と、ノンドープ型又はｎ型ＧａＡｓ基板を除去する工程とを有しており、ｐ型基板及び厚膜層を使用することなく透明基板型半導体発光素子を作製してるので、高温処理時のｐ型ドーパントの活性層への拡散が抑制され、高い内部量子効率が維持され高輝度の半導体発光素子を得ることが可能になる。更に、ＧａＡｓ基板がｎ型である場合は、ｎ型ＧａＡｓ基板上にエピタキシャル成長するｐ型半導体層からのＧａＡｓ基板へのｐ型ドーパントの拡散が抑制されるので、ｐ型電極のオーミックコンタクトが得られ易く、ｐ型半導体層の抵抗率も低く維持されるので、より動作電圧の低い半導体発光素子を得ることが可能になる。

【００５１】従って、ＧａＡｓ基板とＧａＰ基板とが共にｐ型基板を使用して製造した場合の半導体発光素子の外部量子効率は、光吸収基板を用いた構造のものよりも低下するが、ノンドープ型ＧａＡｓ基板とｎ型ＧａＰ基板を使用する場合は、複数の半導体層のエピタキシャル成長時やＧａＡｓ基板上のｎ型ＧａＰキャップ層とｎ型ＧａＰ基板の接合時の高温における、ｐ型ドーパントの発光層への拡散による発光効率の低下は最小限度に抑えられており、外部量子効率は向上する。故に、ノンドープ型ＧａＡｓ基板とｎ型ＧａＰ基板とを使用する場合の、ドーパントの拡散を抑制する効果は十分大きい。また、ｎ型ＧａＡｓ基板を使用する場合は、エピタキシャル成長時の高温におけるｐ型半導体層からｎ型ＧａＡｓ基板中へのｐ型ドーパントの拡散が抑制されるので、抵抗率が低く維持される。従って、ｐ型電極を形成する部分のｐ型半導体層表面のアクセプタ濃度を高く保つことができ、容易にオーミックコンタクトが得られるので、従来に比べ動作電圧の低下が実現できる。

【００５２】また、ｎ型ＧａＰ厚膜層を形成する行程が、ｎ型半導体層上にｎ型ＧａＰ基板を配設する行程と、ｎ型ＧａＰ基板を高温処理によりｎ型半導体層上面に接合する行程とを有しており、ｎ型ＧａＰ基板を高温処理によりｎ型半導体層上面に接合形成しているので、十分に厚いｎ型ＧａＰ基板を容易に作製することができ、ウエハー割れによる処理歩留の低下を防ぐことが可能になる。

【００５３】従って、従来のｐ型ＧａＰ基板を接合形成する場合に比べ、価格の安価なｎ型ＧａＰ基板を利用できるので、製品歩留の向上とあわせ製造コストが大幅に低減できる。

【００５４】また、ｎ型半導体層上にｎ型ＧａＰ厚膜層をエピタキシャル成長で形成しているので、半導体基板を整合する方法に比べて更に製造工程を簡略化することができるので、より効率良く半導体発光素子を製造することが可能になる。

【００５５】従って、例えばウエハー表面のポリッシュ

工程の省略や、n型GaP基板は使用せず価格の安価なn型のGaAs基板のみを使用する等、製造コストが大幅に低減できる。

【0056】また、ノンドープ型又はn型GaAs基板上に積層する単層あるいは複数層からなるp型半導体層が、少なくとも発光層からの光の発光波長に対して透明な電流拡散層を備え、更に電流拡散層は$Al_xGa_{1-x}As$（$0.6<x<0.9$）層、$(Al_yGa_{1-y})_zIn_{1-z}P$（$0 \leqq y \leqq 1$、$0 \leqq z \leqq 1$）、GaP層の中から選ばれた単層あるいは複数層により形成されているので、p型電極からの電流が拡散しやすくなり、p型電極に吸収される光を減少させることが可能になる。

【0057】従って、発光層全体に電流を注入できるので、発光層からの光の外部出射効率が向上する。更に、$(Al_yGa_{1-y})_zIn_{1-z}P$（$0 \leqq y \leqq 1$、$0 \leqq z \leqq 1$）、GaP層は$Al_xGa_{1-x}As$（$0.6<x<0.9$）層に比べてAl含有量が少ないので耐湿性を向上することが可能になる。

【0058】また、ノンドープ型又はn型GaAs基板上に少なくとも$(Al_yGa_{1-y})_zIn_{1-z}P$（$0 \leqq y \leqq 1$、$0 \leqq z \leqq 1$）層又はGaP層を形成後に$Al_xGa_{1-x}As$（$0.6<x<0.9$）層を形成しているので、耐湿性を向上することが可能になる。

【0059】従って、高温、高湿下での半導体発光素子の光度劣化が小さくなり、信頼性が向上する。

【図面の簡単な説明】

【図1】（a）乃至（c）は、本発明の第1の実施の形態において形成された半導体発光素子の側面図、上面図及び底面図。

【図2】（a）乃至（c）は、本発明の第1の実施の形態による半導体発光素子の製造方法を示す工程図。

【図3】（a）乃至（c）は、本発明の第2の実施の形態において形成された半導体発光素子の側面図、上面図及び底面図。

【図4】（a）乃至（c）は、本発明の第2の実施の形態による半導体発光素子の製造方法を示す工程図。

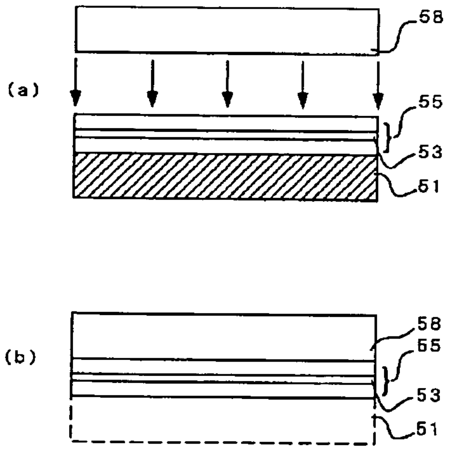
【図5】（a）又は（b）は、従来例による半導体発光素子の製造方法を示す工程図。

【図6】（a）乃至（c）は、他の従来例による半導体発光素子の製造方法を示す工程図。

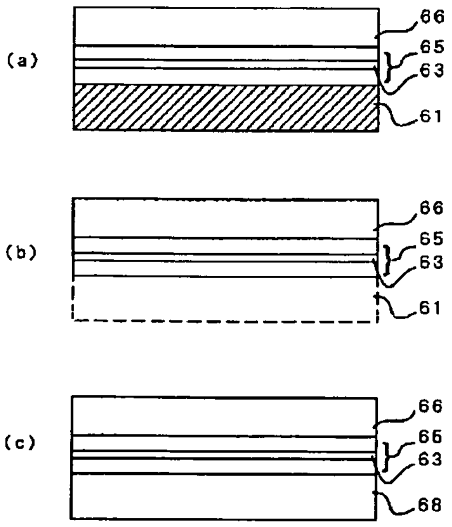
【符号の説明】

1	n型GaP基板
2、32	n型GaPキャップ層
3、33	n型$(Al_{0.2}Ga_{0.8})_{0.77}In_{0.23}P$中間層
4、34	n型$Al_{0.5}In_{0.5}P$クラッド層
5	p型$Ga_{0.5}In_{0.5}P$活性層
6、36	p型$Al_{0.5}In_{0.5}P$クラッド層
7	p型$Al_{0.68}Ga_{0.32}As$電流拡散層
10	ノンドープ型GaAs基板
11、42	p型GaAsバッファー層
31	n型GaP成長層
35	p型$(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P$活性層
37	p型$Al_{0.7}Ga_{0.3}As$電流拡散層
38	p型$(Al_{0.5}Ga_{0.5})_{0.5}In_{0.5}P$保護層
41	n型GaAs基板
100、200	半導体発光素子

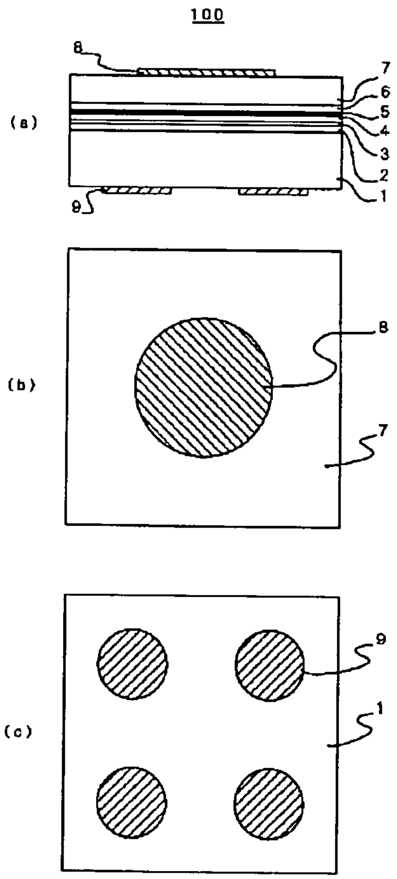
【図5】



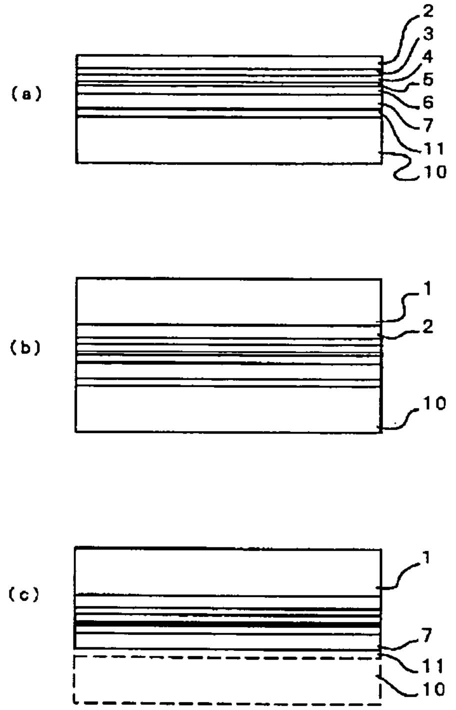
【図6】



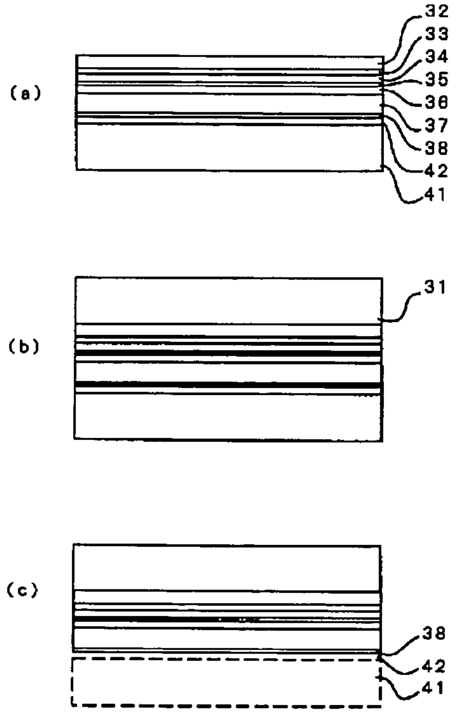
【図1】


(a)
(b)
(c)

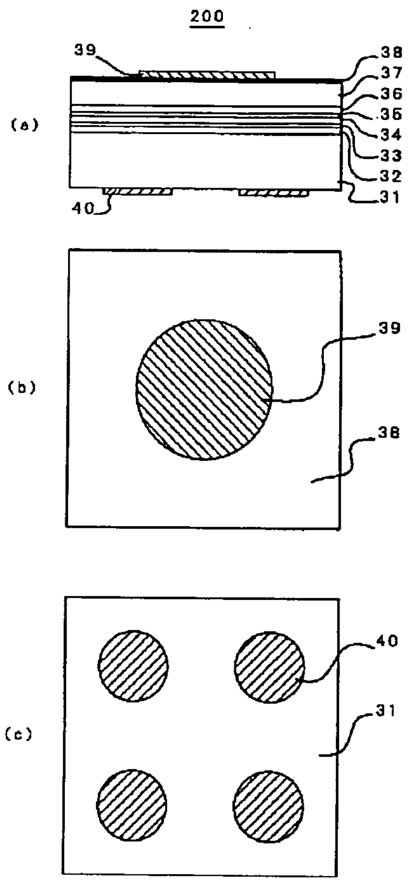
【図2】


(a)
(b)
(c)

【図4】


(a)
(b)
(c)

【図3】



フロントページの続き

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